What is claimed is:

1. A memory cell, comprising:

a source region in a horizontal substrate;

a drain region in the horizontal substrate;

a channel region separating the source and the drain regions;

a vertical floating gate located above a portion of the channel region and separated from the channel region by a first thickness insulator material; and

at least one vertical control gate located above another portion of the channel region and separated therefrom by a second thickness insulator material, wherein the at least one vertical control gate is parallel to and opposing the vertical floating gate, and wherein the at least one vertical control gate is separated from the vertical floating gate by an intergate dielectric.

2. The memory cell of claim 1, wherein the at least one vertical control gate has a horizontal width of approximately 100 nanometers (nm).

3. The memory cell of claim 1, wherein the first thickness insulator material is approximately 60 Angstroms (Å), and wherein the second thickness insulator material is approximately 100 Angstroms (Å).

4. The memory cell of claim 1, wherein the first thickness insulator material, the second thickness insulator material, and the intergate dielectric include silicon dioxide (SiO_2).

5. The memory cell of claim 1, wherein the vertical floating gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 Angstroms (Å).

6. The memory cell of claim 1, wherein the intergate dielectric has a thickness approximately equal to the first thickness insulator material.

7. A transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a vertical floating gate separated from a first portion of the channel region by a first oxide thickness; and

at least one vertical control gate separated from a second portion of the channel region by a second oxide thickness, wherein the at least one vertical control gate is parallel to and opposing the vertical floating gate.

8. The transistor of claim 7, wherein the vertical floating gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 nanometers (nm).

9. The transistor of claim 7, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

10. The transistor of claim 7, wherein the at least one vertical control gate has a horizontal width of approximately 100 Angstroms (Å).

11. The transistor of claim 7, wherein the vertical floating gate separated from a first portion of the channel region includes a first portion of the channel region which is adjacent to the source region, and wherein the at least one vertical control gate separated from a second portion of the channel region includes a second portion of the channel region which is adjacent to the drain region.

12. The transistor of claim 11, wherein the at least one vertical control gate further includes a horizontal member located above the vertical floating gate, wherein the at least one vertical control gate an the horizontal member are separated from the vertical floating gate by an intergate dielectric.

13. The transistor of claim 7, wherein a capacitance between the at least one vertical control gate and the floating gate is greater than a capacitance between the floating gate and the channel.

14. A floating gate transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first vertical gate located above a first portion of the channel region and separated from the channel region by a first oxide thickness;

a second vertical gate located above a second portion of the channel region and separated from the channel region by a second oxide thickness; and

a third vertical gate located above a third portion of the channel region and separated from the channel region by the second oxide thickness.

15. The floating gate transistor of claim 14, wherein the second and the third vertical gates are parallel to and on opposing sides of the first vertical gate.

16. The floating gate transistor of claim 14, wherein the first vertical gate includes a floating gate and wherein the second and the third vertical gates include control gates.

17. The floating gate transistor of claim 14, wherein first vertical gate includes a control gate and wherein the second and the third vertical gates include floating gates.

18. The floating gate transistor of claim 14, wherein the floating gate transistor further includes a horizontal gate member which couples the second and the third vertical gates.

19. The floating gate transistor of claim 14, wherein a greater percentage of a voltage applied to the second and the third vertical gates appears between the first vertical gate and the channel than between the first vertical gate and the second and the third vertical gates.

20. The floating gate transistor of claim 14, wherein the second and the third portion of the channel region are adjacent the source region and the drain region, respectively.

21. The floating gate transistor of claim 14, wherein the first vertical gate, the second vertical gate, and the third vertical gate include polysilicon gates which are separated from one another by silicon dioxide (SiO_2).

22. The floating gate transistor of claim 14, wherein the first vertical gate, the second vertical gate, and the third vertical gate each have a horizontal width of approximately 100 nanometers (nm).

23. The floating gate transistor of claim 14, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

24. A memory device, comprising:

a plurality of memory cells, wherein each memory cell includes:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first vertical gate separated from a first portion of the channel region by a first oxide thickness; and

a second vertical gate separated from a second portion of the channel region by a second oxide thickness, wherein the second vertical gate is parallel to and opposing the first vertical gate; and

at least one sense amplifier, wherein the at least one sense amplifier couples to the plurality of memory cells.

25. The memory device of claim 24, wherein each memory cell includes a flash memory cell.

26. The memory device of claim 24, wherein each memory cell includes an electronically eraseable and programmable read only memory (EEPROM) cell.

27. The memory device of claim 24, wherein the first vertical gate includes a floating gate and the second vertical gate includes a control gate.

28. The memory device of claim 24, wherein the first vertical gate includes a control gate and the second vertical gate includes a floating gate.

29. The memory device of claim 24, wherein the first vertical gate and the second vertical gate have a horizontal width of approximately 100 nanometers (nm).

30. The memory device of claim 24, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

31. The memory device of claim 24, wherein the first vertical gate separated from a first portion of the channel region by a first oxide thickness includes a first portion of the channel region which is adjacent to the source region.

32. The memory device of claim 24, wherein the second vertical gate separated from a second portion of the channel region by a second oxide thickness includes a second portion of the channel region which is adjacent to the source region.

33. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes a plurality of memory cells coupled to at least one sense amplifier, and wherein each memory cell includes:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first vertical gate separated from a first portion of the channel region by a first oxide thickness; and

a second vertical gate separated from a second portion of the channel region by a second oxide thickness, wherein the second vertical gate is parallel to and opposing the first vertical gate.

34. The electronic system of claim 33, wherein each memory cell includes a flash memory cell.

35. The electronic system of claim 34, wherein each memory cell further includes a third vertical gate separated from a third portion of the channel region by the second oxide thickness, and wherein the second and the third vertical gates are parallel to and on opposing sides of the first vertical gate.

36. The electronic system of claim 35, wherein the first vertical gate, the second vertical gate, and the third vertical gate include polysilicon gates which are separated from one another by silicon dioxide (SiO_2).

37. The electronic system of claim 34, wherein the first vertical gate includes a floating gate and the second vertical gate includes a control gate.

38. The electronic system of claim 34, wherein the first vertical gate includes a control gate and the second vertical gate includes a floating gate.

39. The electronic system of claim 34, wherein the first vertical gate and the second vertical gate have a horizontal width of approximately 100 nanometers (nm).

40. The electronic system of claim 34, wherein the first oxide thickness is approximately equal to an intergate dielectric thickness which separates the first vertical gate and the second vertical gate.

41. The electronic system of claim 34, wherein the second vertical gate separated from a second portion of the channel region by a second oxide thickness includes a second portion of the channel region which is adjacent to the source region.

42. The electronic system of claim 34, wherein the first vertical gate further includes a horizontal member located above the second vertical gate.

43. The electronic system of claim 34, wherein a capacitance between the first vertical gate and the second vertical gate is greater than a capacitance between either the first vertical gate or the second vertical gate and the channel.

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44. A method for forming a memory cell, comprising:

forming a source region and a drain region separated by a channel region in a horizontal substrate;

forming a first vertical gate above a first portion of the channel region and separated from the channel region by a first oxide thickness (t1); and

forming a second vertical gate above a second portion of the channel region and separated from the channel region by a second oxide thickness (t2), wherein forming the second vertical gate includes forming the second vertical gate parallel to and opposing the first vertical gate.

45. The method of claim 44, wherein the method further includes forming a flash memory cell.

46. The method of claim 44, wherein forming the first vertical gate includes forming a floating gate, and wherein forming the second vertical gate includes forming a control gate.

47. The method of claim 44, wherein forming the first vertical gate and forming the second vertical gate include forming the first and the second vertical gates to have a horizontal width of approximately 100 nanometers (nm).

48. The method of claim 44, wherein forming a first vertical gate separated from the channel region by a first oxide thickness (t1) includes forming the first vertical gate separated from the channel region by a first oxide thickness (t1) of approximately 60 Angstroms (Å).

49. The method of claim 44, wherein forming a second vertical gate separated from the channel region by a second oxide thickness (t2) includes forming the second vertical gate separated from the channel region by a second oxide thickness (t2) of approximately 100 Angstroms (Å).

50. The method of claim 44, wherein forming the first vertical gate separated from a first portion of the channel region by a first oxide thickness (t1) includes forming the first vertical gate separated from a first portion of the channel region which is adjacent to the source region.

51. The method of claim 44, wherein forming the second vertical gate separated from a second portion of the channel region by a second oxide thickness includes forming the second vertical gate separated from a second portion of the channel region which is adjacent to the source region.

52. A method for forming a floating gate transistor, comprising:

forming a source region and a drain region separated by a channel region in a horizontal substrate;

forming a first vertical gate located above a first portion of the channel region and separated from the channel region by a first oxide thickness;

forming a second vertical gate located above a second portion of the channel region and separated from the channel region by a second oxide thickness; and

forming a third vertical gate located above a third portion of the channel region and separated from the channel region by the second oxide thickness.

53. The method of claim 52, wherein forming the second and the third vertical gates includes forming the second and the third vertical gates parallel to and on opposing sides of the first vertical gate.

54. The method of claim 52, wherein forming the first vertical gate includes forming a floating gate and wherein forming the second and the third vertical gates includes forming control gates.

55. The method of claim 52, wherein forming the first vertical gate includes forming a control gate and wherein forming the second and the third vertical gates includes forming floating gates.

56. The method of claim 52, wherein forming the floating gate transistor further includes forming a horizontal gate member which couples the second and the third vertical gates.

57. The method of claim 52, wherein forming the second and the third vertical gates over a second and a third portion of the channel region, respectively, includes forming the second and the third vertical gates adjacent to the source region and the drain region, respectively.

58. The method of claim 52, wherein forming the first, the second, and the third vertical gates includes forming polysilicon gates which are separated from one another by silicon dioxide (SiO_2).

59. The method of claim 52, wherein forming the first, the second, and the third vertical gates includes forming each gate to have a horizontal width of approximately 100 nanometers (nm).

60. The method of claim 52, wherein forming a first vertical gate separated from the channel region by a first oxide thickness includes forming a first oxide thickness of approximately 60 Angstroms (Å), and wherein forming a second vertical gate

separated from the channel region by a second oxide thickness includes forming a second oxide thickness of approximately 100 Angstroms (Å).

61. A method for operating a memory cell, comprising:

applying a first potential across a thin tunneling oxide between a vertical floating gate and a first portion of a horizontal substrate, the horizontal substrate including a source region and a drain region separated by a horizontal channel region, in order to add or remove a charge from the floating gate; and

reading the memory cell by applying a second potential to a vertical control gate located above a second portion of the horizontal substrate, wherein the vertical control gate is parallel to and opposing the vertical floating gate.

62. A method for operating a memory cell, comprising:

writing a charge from a horizontal substrate to a vertical floating gate by applying a first potential to a vertical control gate;

erasing a charge from a vertical floating gate to a source region in a horizontal substrate by applying a second potential to the vertical control gate; and

reading the memory cell by applying a third potential to the vertical control gate.

63. The method of claim 62, wherein applying a first, second, and third potential to the vertical control gate includes applying a first, second, and third potential to a vertical control gate which is parallel to and opposing the vertical floating gate.

64. The method of claim 62, wherein writing a charge from a horizontal substrate to a vertical floating gate by applying a first potential to a vertical control gate includes tunneling electrons from a horizontal channel in the horizontal substrate to the vertical floating gate using Fowler Nordheim tunneling.

65. The method of claim 62, wherein writing a charge from a horizontal substrate to a vertical floating gate by applying a first potential to a vertical control gate includes using a hot electron injection technique to tunnel electrons at a drain region in the horizontal substrate to the vertical floating gate.

66. The method of claim 62, wherein erasing a charge from a vertical floating gate to a source region in a horizontal substrate by applying a second potential to the vertical control gate includes tunneling electrons from the vertical floating gate to the source region in a horizontal substrate using Fowler Nordheim tunneling.

67. A method for operating a memory cell, comprising:

using a vertical control gate to add and remove a charge to a vertical floating gate; and

using the charge stored on the vertical floating gate to modulate a horizontal conduction channel beneath the vertical floating gate.

68. The method of claim 67, wherein method further includes sensing a conduction level through the horizontal channel to sense a state of the memory cell, wherein the conduction level is modulated by a charge level in a vertical floating gate.

69. A method for operating a memory cell, comprising:

storing a charge in a vertical floating gate; and

using the charge stored in the vertical floating gate to control a threshold voltage level to create conduction in a horizontal channel region beneath the vertical floating gate.